HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

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PATENT APPLICATION

ATTORNEY DOCKET NO. 10990815-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Josh Hogan

Confirmation No.: 4699

Application No.: 09/615,646

Examiner: M. Battaglia

Filing Date: 7/13/2000

Group Art Unit: 2652

Title: PHASE DISCONTINUITY COMPENSATION IN A BIT-ACCURATE OPTICAL DRIVE

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **Feb. 2, 2005**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Typed Name: Hugh Gortler

Signature: [signature]

Rev 12/04 (Aplbrief)

Respectfully submitted,

Josh Hogan

By [signature]

Hugh Gortler

Attorney/Agent for Applicant(s)
Reg. No. **33,890**

Date: **March 17, 2005**

Telephone No.: **(949) 454-0898**

Patent
Docket No. 10990815-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

APPEAL NO. ____________________

In re Application of:
Josh Hogan

Serial No. 09/615,646
Filed: July 13, 2000

Confirmation No. 4699
Examiner: M. Battaglia
Art Unit: 2652

For: **PHASE DISCONTINUITY COMPENSATION IN A BIT-ACCURATE OPTICAL DRIVE**

APPEAL BRIEF

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents Washington, D.C. 20231 on March 17, 2003.

HUGH P. GORTLER, Reg. No. 33,890

Hugh P. Gortler, Esq.

Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

(949) 454-0898

INDEX

1. REAL PARTY IN INTEREST

The real party in interest is the assignee, Hewlett-Packard Company.

2. RELATED APPEALS AND INTERFERENCES

No appeals or interferences are known to have a bearing on the Board's decision in the pending appeal.

3. STATUS OF CLAIMS

Claims 1-26 are pending.

Claim 20 is objected to.

Claims 1-19 and 21-26 are rejected.

The rejections of claims 1-19 and 21-26 are being appealed.

4. STATUS OF AMENDMENTS

No amendment was filed subsequent to final rejection.

5. SUMMARY OF CLAIMED SUBJECT MATTER

"Read/write" optical discs include optical discs that allow data to be written only once and optical discs that allow data to be written many times. A DVD+RW disc is a type of read/write disc that allows data to be written many times.

Figure 1 of the application illustrates a read/write disc 10 with a spiral groove 12 (see also page 4, lines 19-23). Data is written to the read/write disc 10 in the form of blocks 50 Data blocks are usually written in the spiral groove (page 6, lines 4-5).

As shown in Figures 4 and 5 and discussed on page 5, lines 9-22, a typical data block 50 includes sixteen data sectors 52. Each data sector 52 includes header 54 and user data 56. The header 54 includes a sector address (ID) and an error detection code (IED). The user data might include programs, music video or any other type of randomized data.

The spiral groove 12 has a wobble, which allows a bit-accurate drive to determine addresses of data blocks stored on the disc (see Figure 2 and page 4, line 27 to page 5, line 4).

Consider the scenario where data blocks are written to the disc during a first session, and additional data blocks are written to the disc later during a second session. The data blocks written during the first session are referred to as "old" data, and the data blocks written to the disc during the second session are referred to as "new" data.

A phase discontinuity can be created between the old data and the new data. The phase discontinuity is illustrated in Figure 3, and described on page 1, line 30 to page 2, line 4. The new data is written to the right of a block boundary (BB). Marks in solid represent the new data actually written to the disc. Marks in phantom represent locations with the correct phase.

Prior art data recovery circuits include phase-locked loops (PLLs) for locking read clocks to user data. These circuits might not be able to tolerate phase discontinuities during readback of the old data and the new data, because the phase-locked loops cannot recover immediately from these discontinuities. It might take hundreds of clock cycles for the phase-locked loops to recover. User data would be lost while the phase-locked loops are recovering.

The prior art suggests the use of “edit gaps” to overcome the problems resulting from these discontinuities. Edit gaps are spaces that separate data blocks. These spaces give the phase-locked loops time to recover before readback of the new data. However, edit gaps have their drawbacks (e.g., they reduce disc storage capacity).

The problems resulting from phase discontinuities are overcome <u>without the use of edit gaps</u> by the method of claim 1, the bit-accurate drive of claim 15, the apparatus of claim 16, and the apparatus of claim 26.

<u>Independent claim 1</u>

Claim 1 recites a method of reading a block (52) of data stored on an optical disc (10). The method comprises synthesizing header information for the data block (block 104 in Figure 6, and page 6, lines 16-20); recovering actual header information from the disc (block 106 in Figure 6, and page 6, lines 21-23); and recovering actual user data from the disc (block 110 in Figure 6, and page 6, line 29), the user data being phase-shifted by a phase difference between the synthesized and recovered header information (blocks 108 and 112 in Figure 6 and page 6, line 30 to page 7, line 6).

<u>Independent claim 15</u>

Claim 15 recites a bit-accurate read/write drive for reading a data block from a disc. Reference is made to Figure 8. The drive comprises means for synthesizing header information for the data block (block 24 in Figure 8 and page 9, lines 26-30); means for recovering actual header information from the disc (block 28 in Figure 8 and page 9, lines 4-5); and means for recovering actual user data from the disc (block 28 in Figure 8 and page 9, lines 4-5). The user data is

phase-shifted by a phase difference between the synthesized and actual header information (block 24 in Figure 8 and page 10, lines 1-23).

Independent claim 16

Claim 16 recites apparatus for reading a block of data from an optical disc. The apparatus comprises an optical pickup unit (block 22 in Figure 8, and page 8, lines 12-15); an address detector (block 24 in Figure 8 and page 8, lines 18-21); and a data recovery circuit (block 28 in Figure 8 and page 9, lines 4-5) for recovering data from an output of the optical pickup unit. The recovered data includes actual header information (block 54 in Figure 4) and actual user data (block 56 in Figure 4) of the data block. The apparatus further comprises a first circuit (block 210 in Figure 9 and page 9, lines 26-30) for synthesizing header information for the data block; a second circuit (block 212 in Figure 9 and page 10, lines 1-8) for determining a phase difference between the recovered actual header and synthesized header information; and a third circuit (blocks 214-216 in Figure 9, and page 10, lines 9-22) for phase-shifting the recovered user data by the determined phase difference.

Independent claim 26

Claim 26 recites apparatus for correcting a signal recovered during a read operation on a data block stored on a disc. The recovered signal includes actual header information and actual user data of the data block. The apparatus comprises a first circuit (block 210 in Figure 9 and page 9, lines 26-30) for synthesizing header information for the data block; a second circuit (block 212 in Figure 9 and page 10, lines 1-8) for determining a phase difference between the recovered and synthesized header information; and a third circuit (blocks 214-216 in Figure 9, and page 10, lines 9-22) for phase-shifting the recovered user data by the determined phase difference.

By synthesizing header information, recovering actual header information, and using the phase difference between the two to phase shift the user data, recovery from phase discontinuities is immediate. Edit gaps are not needed.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3, 5-9, 14-18, 21 and 26 are rejected under 35 USC §102(b) as being anticipated by Kobayashi U.S. Patent No. 5,835,461.

7. ARGUMENTS

REJECTION UNDER 35 U.S.C §102(b) OVER KOBAYASHI U.S. PATENT NO. 5,835,461

An annotated advisory action is provided in Evidence Appendix A. Kobayashi is provided in Evidence Appendix C.

Kobayashi's figure 1 shows an optical disc 1 with a spiral pregroove 2. The spiral pregroove 2 has a wobble that it "meanders" from side to side in a predetermined cycle. Sync marks are formed in the pregroove 2 (see col. 5, lines 26-28 and 42-43). The wobble and sync marks are used to find addresses on the disc 1. The wobble and sync marks are formed (pre-recorded) in the disc 1 at the time of manufacture (see col. 8, lines 5-10)

At the time of manufacture, the disc 1 contains no user data. It is considered blank. A user can insert the disc 1 in the optical drive of a computer, and add data. According to Kobayashi's scheme, the user data is written to the

disc 1 in clusters. Linking areas, and postambles and postbuffers are used in between clusters of user data (col. 12, lines 5-14). That is, edit gaps are used between clusters of user data.

Figure 14 of Kobayashi show an optical head 32 and a circuit 33 for recording and reproducing data. During a read operation, the optical head irradiates the disc 1 with laser light and senses and reproduces data from the light reflected from the disc (col. 8, lines 15-18). The circuit 33 "suitably demodulates data supplied from the optical head 32 and outputs the demodulated data to [an] unillustrated unit (col. 8, lines 24-26). If the reproduced data contains an address, the address is sent to an address generating and reading circuit 35. Kobayashi also describes data reproduction at col. 10, lines 52-63: the position of the optical head is determined from the output of the address generating circuit 35, reproduced data is stored in memory 34 through the reproducing circuit 33, and eventually read out to an unillustrated unit. Kobayashi doesn't say much more about how the reproduced data is read from the disc 1[1] . Kobayashi does not describe the details of the reproducing circuit 33 or the unillustrated circuit.

Kobayashi does not teach, hint or remotely suggest that the circuit 33 synthesizes header information for a data block; determines a phase difference between the recovered and synthesized header information; and phase-shifts the recovered user data by the determined phase difference. Kobayashi does not even disclose a reproducing circuit 33 that can navigate through phase discontinuities between old data and new data.

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1 Additional description of circuit 33 has to do with write operations, in which data is sent to the optical head 32, which then writes the data to the disc 1.

Instead, Kobayashi appear to address the phase discontinuity problem through the use of edit gaps. These edit gaps, referred to as linking areas, are shown in Figure 19 and described at column 12, lines 5+. Thus, Kobayashi suggests the use of edit gaps, the very thing that the present invention avoids.

In the third office action, the examiner dismissed the discussion of edit gaps because claim 1 doesn't recite the absence of edit gaps. The advisory action elaborates further: "limitations from the specification are not read into the claims" (see annotation A1 on page 2 of the advisory action).

However, the discussion about edit gaps is not directed at claim construction. Rather, the discussion about edit gaps is intended to set up a problem statement. Edit gaps such as those used by Kobayashi have disadvantages. The present invention addresses the problem of phase discontinuities without the use of edit gaps.

The discussion about edit gaps is also intended to highlight the difference between Kobayashi and the present invention. Kobayashi, by using edit gaps, takes a different approach toward addressing phase discontinuities when reading user blocks of data. Kobayashi's edit gaps allow the circuit 33 to recover before the readback of new data. In contrast, the present invention phase-shifts the user data so recovery from phase discontinuities is immediate.

In the advisory action, the '102 rejections are based on elements 36, 37, 40 and 41 of Kobayashi's Figure 14 (see annotation A2 on page 2). However, these elements are used to read <u>pre-recorded address information</u> embedded in the disc 1. These elements are not used to recover data blocks.

Referring to Figure 14 of Kobayashi, a mark detection circuit 36 and a mark cycle detection circuit 40 are used to detect sync marks formed in the wobbled pregroove 2 of the optical disc 1 (col. 6, lines 41-64). If the detected pulses have a constant period, the mark detection cycle detection circuit 40 generates pulses in synchronization with the detected pulses and sends those generated pulses to a phase-locked loop (PLL) 41 (col. 8, lines 55-60). If the detected pulses do not have a constant period, the mark detection circuit 40 generates pseudo-pulses (col. 8, lines 60-64). If the detected pulses are not supplied with a constant period, it is assumed that the detected pulses are not caused by the sync marks. The pseudo pulses prevent the PLL 41 from being locked in an incorrect phase (col. 8, lines 60-64).

The pulses from the mark cycle detection circuit 40 are supplied to the PLL 41. The PLL 41 includes a phase comparator 42 that detects the phase difference between the signal generated by a VCO 44 (via divider 45) and the signal generated by the mark cycle detection circuit 40.

Thus, the elements 36, 37, 40 and 41 do not synthesize header information for a data block, or determine a phase difference between the recovered and synthesized header information, or phase-shift the recovered user data by the determined phase difference. Because Kobayashi does not disclose all features of independent claims 1, 15-16 and 26, the '102 rejections of these claims should be withdrawn. Because Kobayashi does not suggest these features, the independent claims should be allowed over Kobayashi alone.

The '102 rejections should be withdrawn for the additional reason that the claims were given an interpretation that was overbroad. In the advisory action, the examiner contends that actual header information in the claims reads on

Kobayashi's pre-recorded address data and sync marks formed in the disc pregroove (see annotation A3 on page 2), and that the synthesized header information reads on Kobayashi's pseudo pulses (see annotation A4 on pages 2 and 3).

During patent examination, the pending claims must be given their broadest reasonable interpretation consistent with the specification. See, for example, In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000)

The examiner's interpretation of "actual header information" is unreasonable because it ignores ordinary usage, it ignores usage in the specification, it ignores the context of Kobayashi pre-recorded address data and sync marks, and it ignores claim limitations.

In general, a header is a unit of information that precedes a data object (see Evidence Appendix B). According to the specification, a data block header precedes a block of user data. Kobayashi sync marks don't precede a data object, let alone user data. Moreover, the sync marcs do not provide user block information such as ID and IED. Kobayashi's sync marks are not even part of a data block. They are embedded in the wobble of a disc spiral.

The examiner's interpretation of "synthesized header information" is unreasonable because it ignores ordinary usage, it ignores usage in the specification, it ignores the context of Kobayashi pre-recorded address data and sync marks, and it ignores claim limitations. Kobayashi pseudo pulses don't precede a data object, let alone user data. The pseudo pulses do not provide user block information such as ID and IED. Kobayashi's pseudo pulses are not for a data block, they are generated as substitutes for detected sync marks.

The '102 rejections should be withdrawn for the additional reason that the examiner has cited no evidence in the prior art of shifting user data by a phase difference between the synthesized and actual header information. Instead, the examiner substitutes unsubstantiated opinion for evidence.

An examiner's unsubstantiated allegations with respect to knowledge in the prior art does not provide evidence of suggestion, particularly in light of a challenge. See <u>In re Ahlert</u>, 424 F2d.,1088, 1091-92 165 USPQ 418, 420-421 (CCPA1970). The examiner's unsubstantiated allegations were challenged in responses to previous office actions. The unsubstantiated allegations are also challenged below as being based on speculation and flawed technical analysis.

The claims recite that user data is shifted by a phase difference between the synthesized and actual header information. The examiner contends that this feature is disclosed by Kobayashi because Kobayashi discloses that circuits 36, 37, 40 and 41 generate a clock that is supplied to each circuit and to a sector counter that drives a spindle motor A2 on page 2) and that "a shift or adjustment in the timing of the clock inherently produces a corresponding phase shift in the user data produced by the reproducing circuit because the entire system (Fig. 14) is controlled by the clock (see annotation A5 on page 2).

First, Kobayashi does not expressly state that the clock (CLOCK) shifts the user data. Second, Kobayashi does not even disclose how the reproducing circuit 33 uses the clock. The statements about the clock being used to shift user data are sheer speculation (made with the benefit of the present application).

Third, the examiner does not even explain how or why the shift in user data is inherent. Thus, the speculation has holes.

Fourth, the examiner cites a passage at col. 9, lines 12-13 for the proposition that the entire system is controlled by the clock. However, this passage says no such thing. The passage simply says that the clock is supplied to each circuit and to a sector counter. It should be noted that this passage does not identify the circuits by reference numeral.

Fifth, the examiner's speculation is contradicted by Kobayashi. The purpose of the pseudo pulses is to maintain the correct phase. If the detected pulses are not supplied with a constant period, it is assumed that the detected pulses are not caused by sync marks. The pseudo pulses prevent the PLL 41 from being locked in an incorrect phase (col. 8, lines 60-64). Thus, the pseudo pulses are generated to <u>prevent</u> the phase of the clock from being shifted.

For the reasons above, all pending claims should be allowed over Kobayashi alone because Kobayashi does not teach or suggest a method or apparatus for navigating past phase discontinuities by synthesizing header information for a data block, determining a phase difference between the recovered and synthesized header information, and phase-shifting the recovered user data by the determined phase difference. The Honorable Board of Patent Appeals and Interferences is respectfully requested to reverse the rejections over Kobayashi.

Respectfully submitted,

Hugh P. Gortler, Esq.
Attorney for Appellant
Registration No. 33, 890

Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

(949) 454-0898

Date: March 17, 2005

8. CLAIMS APPENDIX

1. (Original) A method of reading a block of data stored on an optical disc, the data block including header information, the method comprising the steps of:

synthesizing header information for the data block;

recovering actual header information from the disc; and

recovering actual user data from the disc, the user data being phase-shifted by a phase difference between the synthesized and recovered header information.

2. (Original) The method of claim 1, wherein the step of synthesizing the header information includes the steps of recovering address information from a wobble embossed on the disc; and synthesizing the header information from the recovered address information.

3. (Original) The method of claim 1, wherein the step of synthesizing the header information includes the steps of obtaining address information from the disc; and synthesizing the header information from the obtained address information.

4. (Original) The method of claim 3, wherein multiple candidates are synthesized from the address; wherein a phase difference between the actual header information and a best candidate is determined; and wherein the recovered user data is shifted according to the determined phase difference.

5. (Original) The method of claim 3, wherein the header information is synthesized by modulation encoding the address information according to a pre-specified format.

6. (Original) The method of claim 1, wherein the synthesized header information includes a sector address.

7. (Original) The method of claim 1, wherein the synthesized header information includes a sector address and an error detection code.

8. (Original) The method of claim 1, wherein a combination of analog and digital techniques are used to phase-shift the recovered user data.

9. (Previously presented) The method of claim 1, wherein a read clock is used to recover the user data; and wherein the recovered user data is phase shifted by creating a phase difference between the read clock and the recovered user data.

10. (Previously presented) The method of claim 9, wherein the recovered user data is phase shifted by time-delaying the recovered user data.

11. (Previously presented) The method of claim 9, wherein the recovered user data is phase-shifted by time-delaying the read clock.

12. (Original) The method of claim 1, wherein the recovered user data is stored in memory prior to demodulation; and wherein the recovered user data is digitally phase-shifted by shifting the data stored in the memory.

13. (Original) The method of claim 1, wherein a phase difference is determined for only the first data sector of the block.

14. (Original) The method of claim 1, wherein a read clock is used to recover the block from the disc; and wherein the phase difference is faded to zero according to a time constant related to the read clock.

15. (Original) A bit-accurate read/write drive for reading a data block from a disc, the drive comprising:

means for synthesizing header information for the data block;

means for recovering actual header information from the disc; and

means for recovering actual user data from the disc, the user data being phase-shifted by a phase difference between the synthesized and actual header information.

16. (Previously presented) Apparatus for reading a block of data from an optical disc, the apparatus comprising:

an optical pickup unit;

an address detector;

a data recovery circuit for recovering data from an output of the optical pickup unit, the recovered data including actual header information and actual user data of the data block;

a first circuit for synthesizing header information for the data block;

a second circuit for determining a phase difference between the recovered actual header and synthesized header information; and

a third circuit for phase-shifting the recovered user data by the determined phase difference.

17. (Original) The apparatus of claim 16, wherein the first circuit synthesizes the header information by recovering address information from a wobble embossed on the disc; and synthesizing the header information from the recovered address information.

18. (Original) The apparatus of claim 16, wherein address information is contained on the disc; and wherein the first circuit synthesizes the header information from the address information contained on the disc.

19. (Original) The apparatus of claim 18, wherein the second circuit generates multiple candidates from the address information and determines the phase difference as the phase difference between the recovered actual header information and a best candidate.

20. (Original) The apparatus of claim 16, wherein the third circuit includes a variable delay for phase-shifting by a fractional portion of the phase difference and memory for shifting by an integer portion of the phase difference.

21. (Original) The apparatus of claim 16, wherein the data recovery circuit includes a read clock; and wherein the recovered actual data is phase-shifted by creating a phase difference between the read clock and the recovered actual user data.

22. (Original) The apparatus of claim 21, wherein the recovered data is phase shifted by time-delaying the recovered actual user data.

23. (Original) The apparatus of claim 21, wherein the recovered data is phase-shifted by time-delaying the read clock.

24. (Original) The apparatus of claim 16, wherein the data recovery circuit includes a read clock; and wherein the second circuit determines a phase difference only for the first data sector of the block and fades the phase difference to zero according to a time constant related to the read clock.

25. (Original) The apparatus of claim 16, wherein the apparatus is a DVD drive.

26. (Original) Apparatus for correcting a signal recovered during a read operation on a data block stored on a disc, the recovered signal including actual header information and actual user data of the data block, the apparatus comprising:

a first circuit for synthesizing header information for the data block;

a second circuit for determining a phase difference between the recovered and synthesized header information; and

a third circuit for phase-shifting the recovered user data by the determined phase difference.

APPENDIX A

Advisory Action	Application No.	Applicant(s)	
	09/615,646	HOGAN ET AL.	
	Examiner	**Art Unit**	
	Michael V Battaglia	2652	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 21 December 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires ______months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1.☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2.☒ The proposed amendment(s) will not be entered because:

(a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

(b) ☐ they raise the issue of new matter (see Note below);

(c) ☒ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

(d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____.

3.☐ Applicant's reply has overcome the following rejection(s): _____.

4.☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5.☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *see attached Response to Arguments*.

6.☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7.☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____.

Claim(s) objected to: *20*.

Claim(s) rejected: *1-19 and 21-26*.

Claim(s) withdrawn from consideration: _____.

8.☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9.☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10.☐ Other: _____

Response to Arguments

Applicant's arguments filed December 21, 2004 have been fully considered but they are not persuasive. In response to Applicant's argument about the irrelevance of the Office action's observation of claim 1's omission of a limitation requiring the absence of edit gaps, the observation is relevant because it points out that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). A1

In response to Applicant's arguments that the rejections confuse user data with pre-recorded address data, there is no confusion on Examiner's end because the pre-recorded address data and sync marks formed in the pregroove of Kobayashi is used to read on the claimed "header information" while only the user data of Kobayashi that is written in clusters is used to read on the claimed "user data". A3 The rejections refer to the circuits of Kobayashi for reading the information in the pre-groove because those circuits (Fig. 14, elements 36, 37, 40 and 41) generate a clock (Fig. 14, CLOCK) that is supplied to each circuit and to a sector counter (Fig. 14, element 46) that is used to drive the spindle motor (Fig. 14, element 31 and Col. 9, lines 12-29). A2 A shift or adjustment in the timing of the clock inherently produces a corresponding phase shift in the user data reproduced by the recording and reproducing circuit (Fig. 14, element 33) because the entire system (Fig. 14) including the recording and reproducing circuit is controlled by the clock (Col. 9, lines 12-13). A5 Thus Examiner asserts neither that there is no difference between user data and pre-recorded address data nor that user data can be read using the circuits for reading the information in the pre-groove.

In regard to Applicant's arguments that Kobayashi does not teach user data being shifted by a phase difference between synthesized and recovered header information, the phase difference

detected by the phase comparator (Fig. 14, element 42) shifts user data by using the phase difference to adjust or shift the phase of the clock used by the recording and reproducing circuit to reproduce user data from the optical disc (Fig. 14, element 1). The phase difference detected by the comparator is between synthesized and recovered header information. The pregroove information including the sync marks read upon the claimed "header information". The mark cycle detection circuit (Fig. 14, element 40) generates pulses in synchronization with detected sync marks and supplies them to the phase comparator if the detected sync marks have constant period (Col. 8, lines 55-60). The phase comparator is part of a phase lock loop (PLL) circuit (Fig. 14, element 41). The PLL adjusts the phase of a clock used for reproduction to have the phase of the pulses generated by the mark cycle detection circuit. Therefore, if the detected sync marks have constant period, the phase of the PLL output matches the phase of the detected sync signals or detected header information. When the detected signals no longer have constant period, the mark cycle detection circuit generates pseudo pulses to replace the pulses synchronized and in phase with the detected sync marks (Col. 8, lines 60-62). The pseudo pulses are synthesized sync marks and, as a result, read upon the claimed "synthesized header information". The detected sync marks read upon the claimed "actual header information". Thus, when the detected sync marks or actual header information is no longer in constant period, the phase of the first pseudo pulse or synthesized header information generated is compared with the phase of the divided PLL output, which is synchronized to the phase of actual header information. The resulting phase difference between synthesized and detected header information shifts user data that is recovered from the disc by adjusting the phase of the clock used by the recording and reproducing circuit to reproduce user data.

A3

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A3

A5

The circuits that read the pre-recorded address information generate the read clock used for reading user information. A shift in the read clock generated by the circuits that read the pre-recorded address information causes a shift in the recovered user data.

The above explanation explains how Kobayashi phase shifts user data based upon a phase difference between actual and synthesized header information. The entire explanation (previous two paragraphs) is connected to user data because the explanation explains how the user data is phase shifted by the claimed phase difference. Further, Examiner thanks Applicant for noting the imprecise phraseology in explaining how Kobayashi reads upon the claimed invention in the explanation above. It is noted that the imprecise phraseology has been corrected.

Applicant's arguments regarding claims 2-19 and 21-26 are unpersuasive because they rely on the unpersuasive arguments that claim 1 is allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael V Battaglia whose telephone number is (703) 305-4534. The examiner can normally be reached on 5-4/9 Plan with 1st Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa T Nguyen can be reached on (703) 305-9687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Battaglia

Michael Battaglia

HOA T. NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600
1/3/05

APPENDIX B

header

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(1) In many disciplines of computer science, a header is a unit of information that precedes a data object. In a network transmission, a header is part of the data packet and contains transparent information about the file or the transmission. In file management, a header is a region at the beginning of each file where bookkeeping information is kept. The file header may contain the date the file was created, the date it was last updated, and the file's size. The header can be accessed only by the operating system or by specialized programs.

(2) In word processing, one or more lines of text that appears at the top of each page of a document. Once you specify the text that should appear in the header, the word processor automatically inserts it.

Most word processors allow you to use special symbols in the header that represent changing values. For example, you can enter a symbol for the page number, and the word processor will automatically replace the symbol with the